ABSTRACT OF THE DISCLOSURE

An apparatus for memory error control coding comprising a first circuit and a second circuit. The first circuit may be configured to generate a multi-bit digital syndrome signal in response to a read data signal and a read parity signal. The second circuit may be configured to (i) detect an error when the bits of the syndrome signal are not all the same state and (ii) generate an error location signal in response the syndrome signal. The error location signal may be generated in response to fewer than all of the bits of the syndrome signal.